PULSONIX

Pulsonix Design System

V2.1 Update Notes

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Printed in the UK. Issue date: 27/10/03 iss 2

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Chapter 1. Getting Started With V2.1

About these notes

These update notes are provided for existing users as a supplement to their existing Pulsonix Users Guide. These notes are to highlight new features in version 2.1 and to briefly describe their use.

Each chapter is broken down into logical functional descriptions based on the application type, Schematic design, PCB design etc.

This is a minor version to release new functionality and service fixes to the field, the previous major release (version 2.0) Update Notes are also included on the installation CD for your reference.

Installing the new version

It is recommended that you back-up all libraries, designs, technology files, profile files, reports and netlists before installing the latest version. Other than for any reason, this is good working practice, although you should have a backup already of all this data!

As with any other installation of Pulsonix, insert the CD and wait for a short time. The *Autorun* facility will start the installation procedure. Follow the on-screen messages from the install wizard. You should install Pulsonix V2.1 on top of your existing installation, you do not need to uninstall any old version first.

There are some small changes to the install procedure that mainly affects the licensing scheme used, whether it is node locked (as it currently is) or whether it is a network license. Network licensing is a new cost option and you can upgrade your existing node locked licensing to this scheme.

For existing users it is recommended that you simply click the **No Change In Licensing** check box on the licensing page of the wizard. Any new licenses and changes to network licensing can be made after the installation using the License Manager.

Chapter 2. General Options

Introduction

This section covers all item changes common to both Schematics, PCB and non-design related options such as the Library Manager or Pulsonix interface.

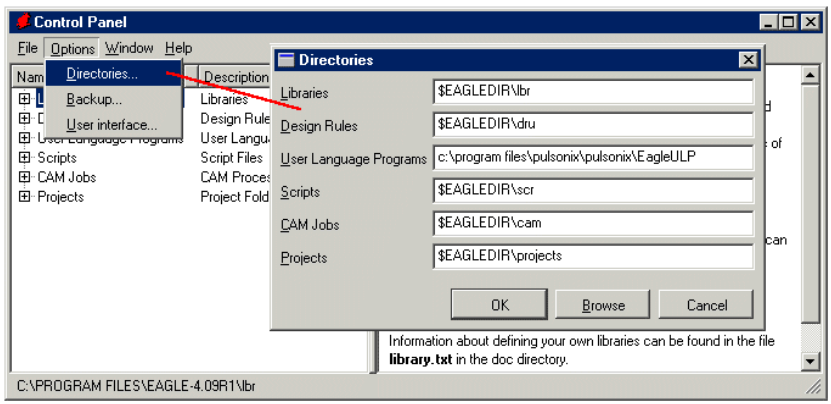
Eagle Importer

Eagle Schematic and PCB designs, Parts, Footprints and Schematic Symbol libraries can be transferred to Pulsonix. Designs and libraries up to and including Eagle Version 4 are supported.

Eagle designs and libraries are held in a binary format, so Pulsonix is supplied with programs that can be run in the Eagle environment. These translate the designs and libraries into an intermediate ASCII format that can be imported into Pulsonix.

For Pulsonix 2.1, a set of Eagle script files (ULP files) is installed into the Pulsonix installation folder under \EagleULP. These are used by the Eagle program when the selection of the ULP file is required.

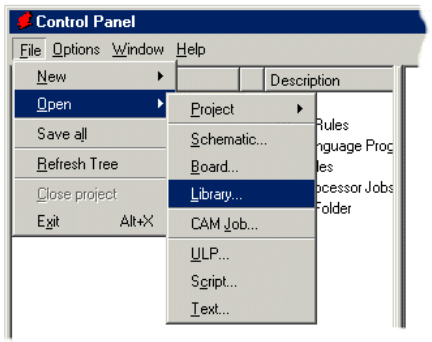
When directed in the text below for the path for the ULP files you can use this facility in one of two ways depending on your preference. The first way is to use it as directed, the second way is to change the default path used in the **Eagle** preferences dialog. From the **Control Panel** window, select the **Options** menu and **Directories**. On the **Directories** dialog, enter the Pulsonix installation path and **EagleULP** folder name.



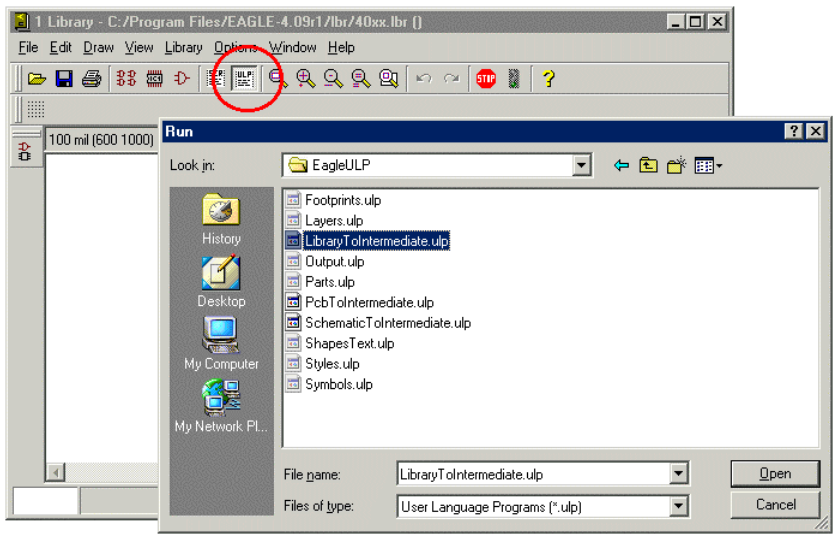
Exporting files

▶ To export Eagle libraries

1. Start the **Eagle Control Panel**
2. From the **File** menu select **Open** and select **Library**.



3. Select the library that you want to transfer.
4. The Library Manager runs up.
5. From the **File** menu select **Run**, this can be run from the toolbar using the icon **ULP**



6. Browse to the EagleULP sub folder of your Pulsonix installation. This folder contains the Eagle to Pulsonix translation programs.
7. Select **LibraryToIntermediate.ulp**

8. A file browser will prompt you for the intermediate file that you want to write to. The name should have the extension **.EIL**
9. This file can then be loaded into Pulsonix, see below.

▶ To export PCB designs from Eagle

1. Start the **Eagle Control Panel**
2. From the **File** menu, select **Open** and **Board**.
3. Open the board that you want to transfer.
4. If the board file is part of a project then the Schematic will also be opened. The Schematic must be kept open as it holds data that the translation program needs.
5. From the **File** menu select **Run**, this can be run from the toolbar using the icon **ULP**
6. Browse to the EagleULP sub folder of your Pulsonix installation. This folder contains the Eagle to Pulsonix translation programs.
7. Select **PCBToIntermediate.ulp**
8. A file browser will prompt you for the intermediate file that you want to write to. The name should have the extension **.EIP**
9. This file can then be loaded into Pulsonix, see below.

▶ To export Schematic designs from Eagle

1. Either switch to the Schematic design program that was opened when the PCB board was opened, or ;
2. Start the **Eagle Control Panel**, from the **File** menu, select **Open** and **Schematic**.
3. Open the Schematic design that you want to transfer.
4. From the **File** menu select **Run**, this can be run from the toolbar using the icon **ULP**
5. Browse to the EagleULP sub folder of your Pulsonix installation. This folder contains the Eagle to Pulsonix translation programs.
6. Select **SchematicToIntermediate.ulp**
7. A file browser will prompt you for the intermediate file that you want to write to. The name should have the extension **.EIS**
8. This file can then be loaded into Pulsonix, see below.

Importing Files

▶ To import the intermediate files into the Pulsonix library

Libraries

1. The PCB and Schematic intermediate files can be read into Pulsonix by using the **File** menu and **Open.**
2. The designs will convert and open in the appropriate design editor.

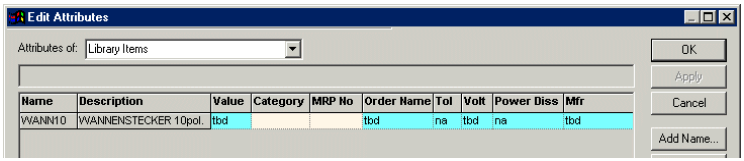
▶ To import the intermediate files into a Pulsonix Design

Designs

1. To create the appropriate libraries from the Eagle library intermediate file, run the Pulsonix Library Manager.
2. From the **Setup** menu select **Libraries**.
3. On each of the **Schematic Symbols**, **PCB Footprints** and **Parts** tabs use **Import** in each library to import the appropriate intermediate file.
4. Once the file has been loaded, the Contents list will display the library.
5. You should convert the Schematic Symbols and PCB Footprints before converting the Parts libraries.
6. Alternatively you can use the Data Transfer Wizard.

Changes to the Attribute Editor

The **Attribute Editor** has been changed so that when using it from the **Library Manager** Parts page, the attribute names in the Technology file are loaded into the grid for use, even if they don't already exist in the Part.



You can now edit the attributes of just the selected items. If some items are selected in a PCB or Schematic design and the Edit Attributes option is used, you now get a warning dialog "Edit attributes of selected items only?". This warning can be turned off once the user is used to it.

Previous In Sequence command

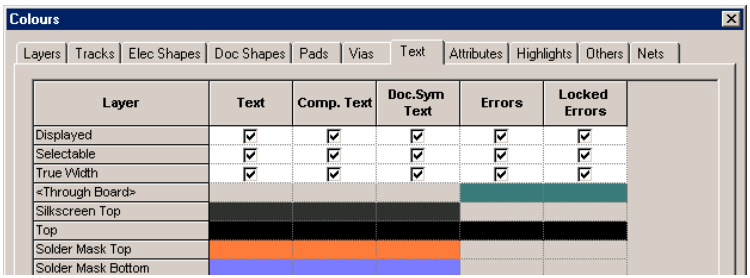
When using the option, **Move From Bin** you can use the command **Previous In Sequence**. This compliments the existing **Next In Sequence** command.

Move From Bin is available when selecting the right mouse menu when in free space on a design and where Components exist in the Component Bin.

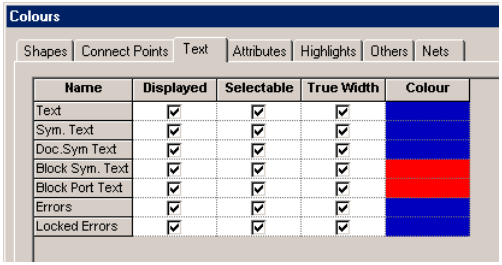
Separate Colours For Locked Errors

On the **Text** tab of the **Colours** dialogs for Schematics and PCB there is a new entry for **Locked Errors**. Any errors which are locked in the design can be easily identified over normal unlocked error markers.

Locked errors are not reported again by the DRC option and retained until unlocked at a later time.

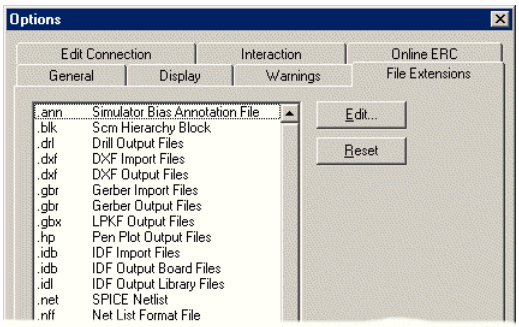


The Schematic Colours dialog looks like this:



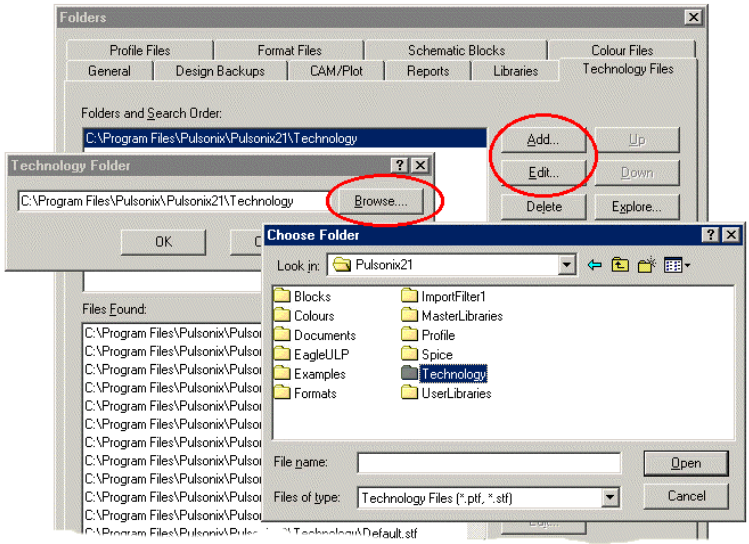
User Defined File Extensions

The **File Extensions** dialog for **Options** now contains the file extensions for the CAM Plot option and for the Import of DXF, IDF and Gerber files.

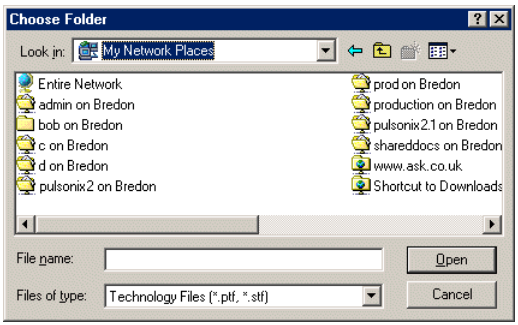


New folder Browser

The **Choose Folders** dialog has been replaced with a more standard Windows folders browser. Available from the **Add** or **Edit** buttons on the **Folders** dialog or **Library Manager Folders** page.

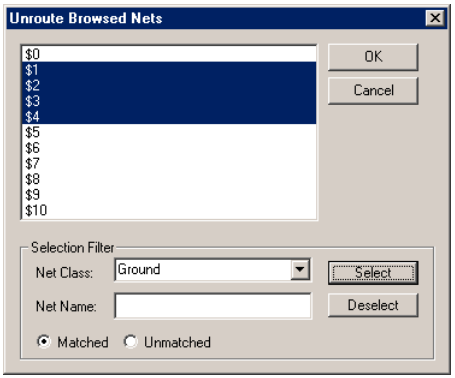


This new dialog also allows easy access to the Network Neighborhood.



Improved Browse Nets Dialog

The **Browse Nets** dialog used in various options has been improved to allow the selection of nets by **Net Class** and **Net Name** using wildcards.



Once the **Selection Filter** criteria have been chosen (using the Net Class and/or Net Name choice), you click the Select button to make the selection in the top part of the window.

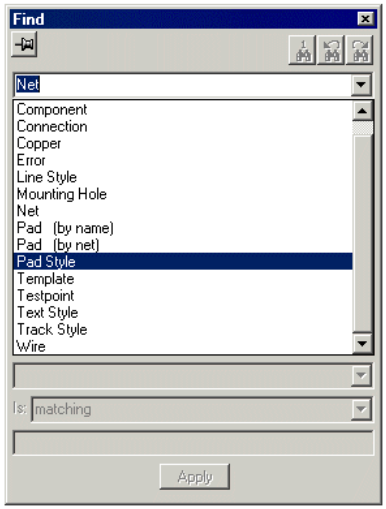
The Selection Filter is accumulative, you can make a selection based on the Ground net class for example, then select another net class of Power for example, then click Select again, both Ground and Power net classes in the list will be selected ready for an action. Likewise, you can also reduce the selection by selecting the **Unmatched** radio button and then **Select**.

Clicking **OK** will then make then apply the appropriate command to the relevant nets.

Find Option Improvements

Find Style

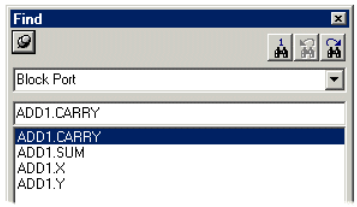
The **Find** option now allows you to find items by their **style** name.



Items can be located by **Styles** for **Lines**, **Pads**, **Text** and **Track**s. This is useful when trying to delete a style from the design to find what used it. Another use is to select all tracks for example that use a particular style, to change them all to a different style.

Find Block Port

In the Schematic Editor, Find can be used for **Block Ports**.



The list presented will include all block ports in the design and their pin numbers/names.

Find Pads by name

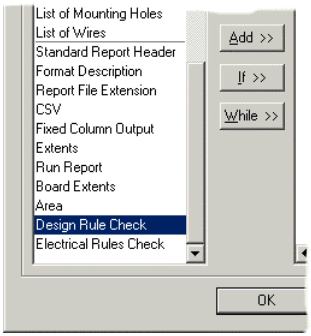
You can now **Find** pads by name using **Pad (by name)** or by net using **Pad (by net)**

In addition to these new Find options, the Find Pads and Find Pins options have been added to the **Edit** menu **Find** option for the respective PCB and Schematics applications.

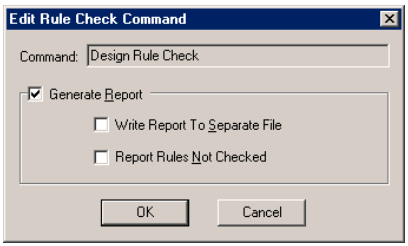
Report Maker Enhancements

Run DRC/ERC options

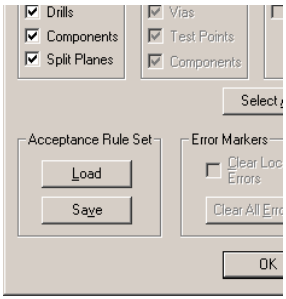
The **Report Maker** option has been enhanced to include the ability to run a **Design Rules Check** from PCB or **Electrical Rules Check** (from Schematics).



When selected you get the following dialog. This allows you to set up report options.



When run, the rules are checked are the **Acceptance Rules Set** saved in the design using the DRC or ERC dialogs.

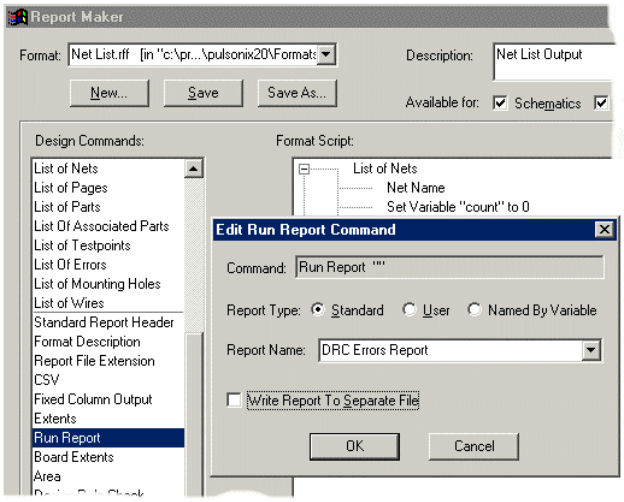


With changes made to both the DRC/ERC dialogs for setting and loading these Acceptance rules, and a change made to the subsequent report which outputs the rules run and the rules not run, you can run a ‘final’ design rules check at the same time as your manufacturing plots.

Running report from within reports

A new Design command allows you to specify the name of a report to run from within the current format script.

You can now produce a sign off report, one that runs the DRC option and several reports. You can now run reports through the CAM plot mechanism.



New fields

For Design level (top level) there are new commands for:

Is PCB Design Is Schematic Design

These are only available if the report is available for SCM & PCB.

New PCB only commands:

Need Back Annotation Is Bin Empty

For the List of Nets command for PCB designs, there is a new command for outputting **Track Length**.

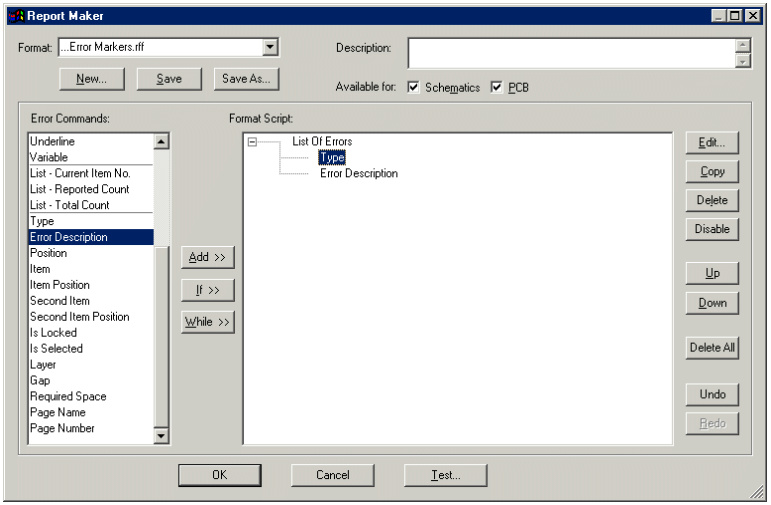
New dialog commands

In addition to the **Delete** button on the dialog, you can use the **Del** key on the keyboard to delete selected commands in the Format Script.

Undo/Redo buttons have been introduced to allow multi-level undo and redo of script editing.

Report design error markers

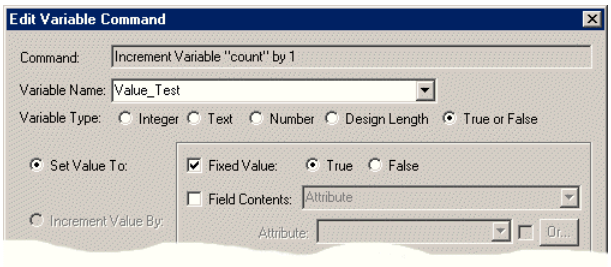
With the introduction of the **List Of Errors** command, you can now extract any design error markers that exist in the Schematic or PCB designs when the report is run.



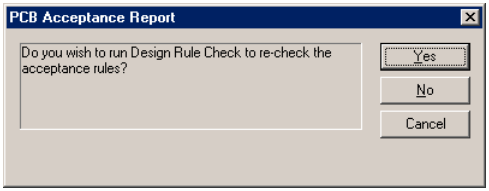
Various Commands exist for the error markers once the List Of Errors command has been used in the format script.

New Variable type

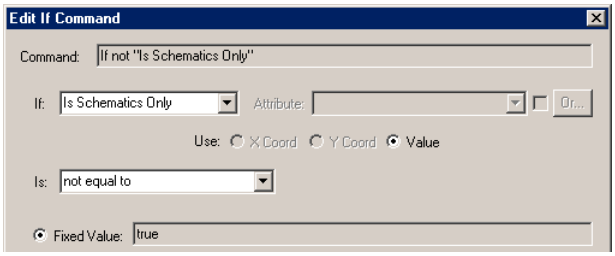
New variable type "True or False".



This allows a better prompt for this type of variable with Yes and No buttons. For example:



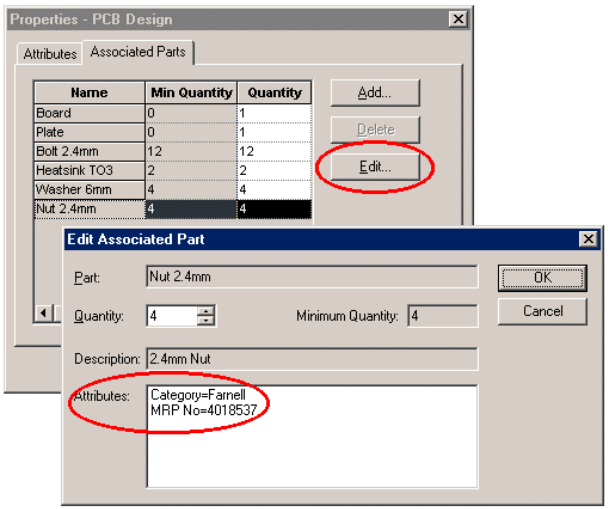
If filed commands are Boolean in nature, then performing an “IF” on them will have a fixed value of “true”. This means you don’t have to type it in. The test can be *not equal to true* or *equal to true*.



Properties for Associated Parts

Associate Parts now display their own **Attributes**. To view these, click on the **Edit** menu and **Design Properties**, then use the **Edit** button for the Associated Part required.

The list of Associate Part Attributes can also be viewed by using the **Report Maker**.

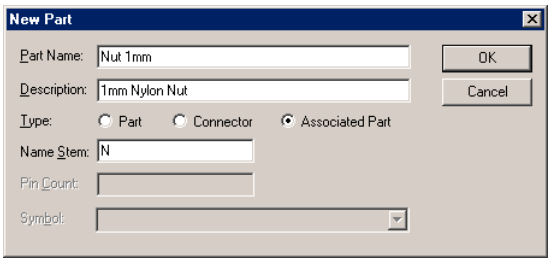


The ability to edit Attributes for Associate Parts is also available from within the Parts Editor.

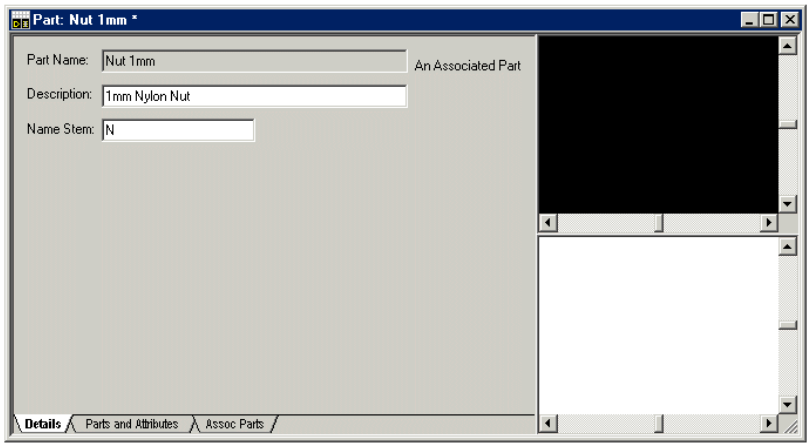
Creating Associated Parts

Part Editor

When creating new Parts, there is a radio button that you specify for Associate Parts.

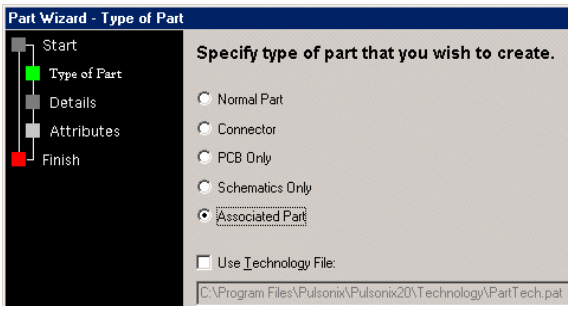


Once in the Part Editor you have no Schematic Symbol or PCB Footprint, and you only have the **Parts and Attributes** and the **Assoc Parts** tabs available.



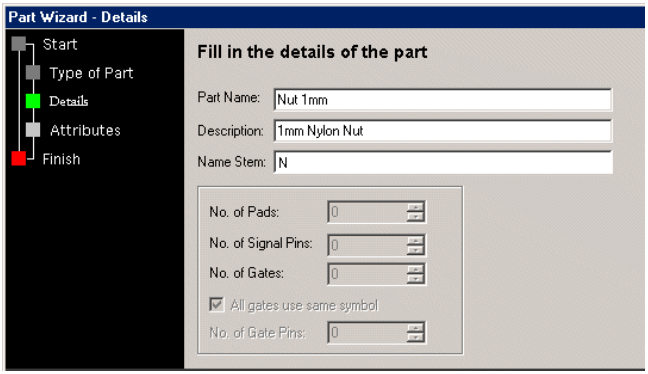
Part Wizard

By selecting the **Associated Part** radio button from the **Part Wizard**, the number of pages for the wizard is reduced to just those required.



Note: The Part Wizard now also contains a new entry for the creation of Schematics Only Parts.

On the **Details** page, the number of pads and gate information is not available.

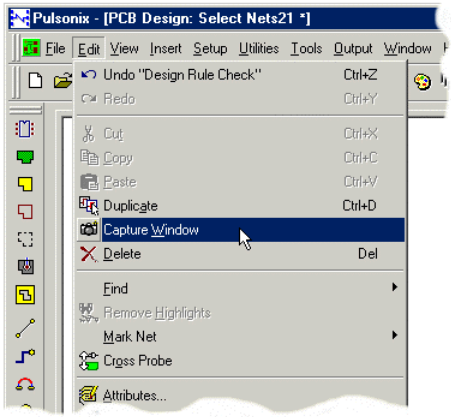


Capture Window

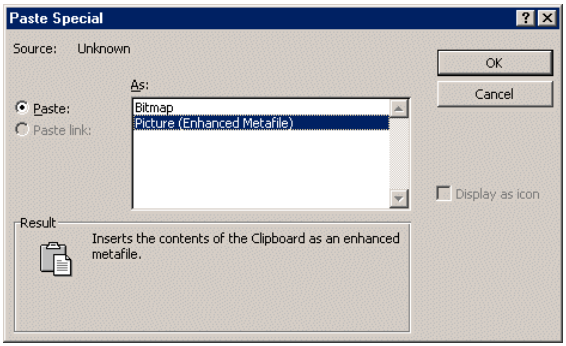
On the **Edit** menu, the Copy To Bitmap command has been replaced by the **Capture Window** command. This will capture the current view to an image in the clipboard.

The standard Copy command, in addition to copying the current selection in native design format, will now also make the selection available on the clipboard as an image.

Once copied to the clipboard, the image is available to paste in either **Windows Bitmap** or a **Windows Metafile** format.



Subsequently, in other applications, either format may be chosen. Microsoft Word for example, will choose to paste Metafile by default but the Paste Special option may be used to explicitly choose the format to paste. For other applications, please refer to that product's users guide.

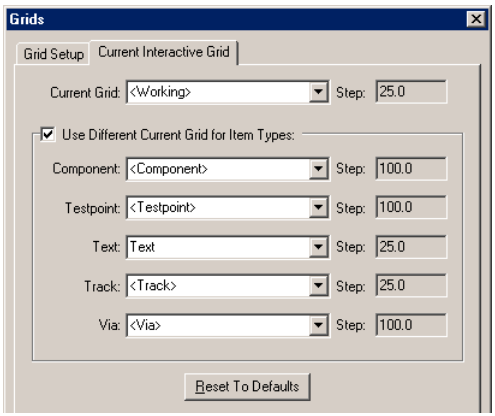


Scaling of vector graphics pictures will incur far less distortion and loss of picture clarity. If possible, always use this format for documentation.

Changes to Grids

There is now a set of current interactive grids for the special items, plus a current interactive grid used for all other items, all saved in the design (or Technology).

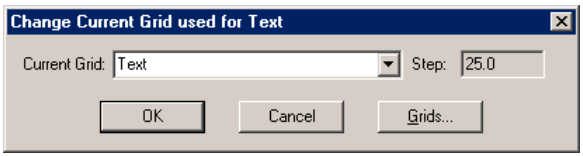
The current interactive grids will be presented to you as a separate page on the grids dialog.



In this dialog you can switch the use of special item grids off (**Use Different Current Grid Item Type**). This way you have just one interactive grid which all items use.

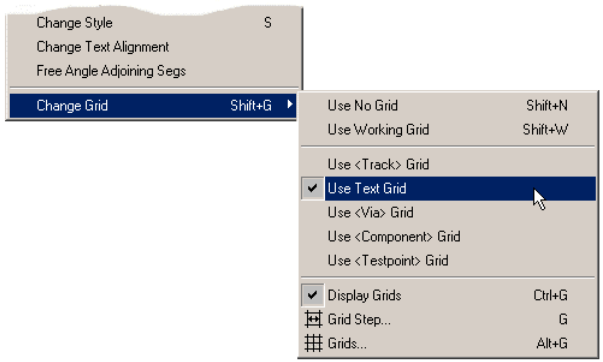
In the design, typing <**G**> at any point puts up the **Change Current Grid** dialog to change the grid currently used for the item type being edited. If the item has a special grid, the title of the dialog will be **Change Current Grid used for Components** for example.

*Note: This dialog has changed from the **Grid Step** dialog in 2.0.*

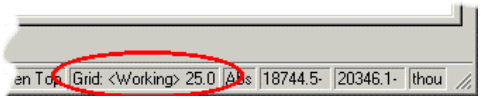


Now if editing text and you change grid to 20 by typing <G20> it does not change the working grid, it changes the current grid used for text items. All text items will now move on this grid in this design.

This change enables you to move items on user named grids. The context menu for change grid will include all user-defined grids. If you pick one it again changes the designs current grid for the item type being edited.

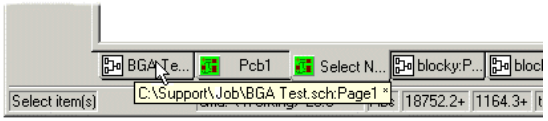


The current grid being used will be displayed on the status bar.

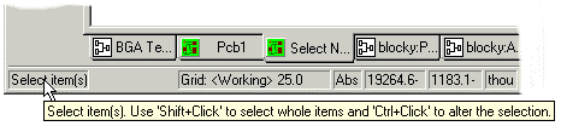


Additional Tooltips

The full library or design path is shown using tooltips when the cursor is over the tab for the Workbook mode. Particularly useful when you have many designs or libraries open at the same time.

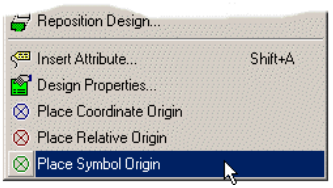


If you make your design window so small that the selected item's properties shown on the Status bar obscure the Prompt message on the status bar, then you can hover over the Prompt and the tooltip will give you the full message.



Place Symbol Origin

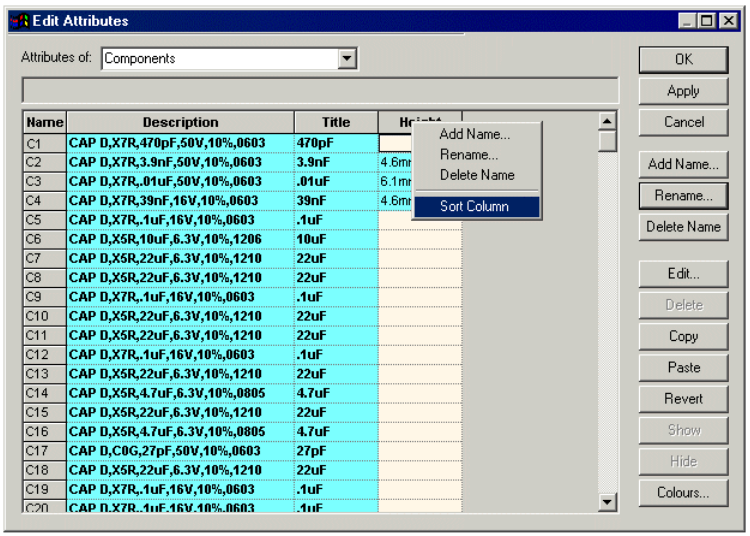
This new option is available on the context menu when editing a Schematic Symbol or PCB Footprint. It should be used if the location of the symbol origin is different to the current one.



Changes to Attribute Editor

There are a number of changes to the Attribute Editor:

- Left click on a column header now selects the whole column.
- Left click on the name cell selects the whole row.
- Right click on a column header will give you a context menu containing **Sort Column** (see below).
- Attribute values that are inherited from another item are drawn in **bold** text.
- The **Delete** button becomes **Reset** if the value has an inherited value it can reset to.
- If you have mixture of selected cells **Delete/Reset** are displayed.

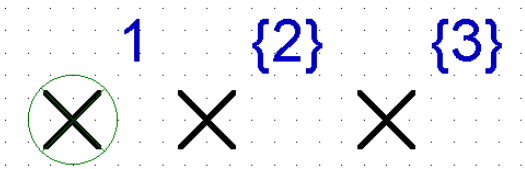


‘Finish Here’ for circle, line & triangle

From the right mouse menu, when adding a circle, line or triangle you can **Finish Here.**

Drawing Pin Names in Symbol Editor

Pin Names which are not displayed in a design, are still drawn in the symbol editor, but the value is shown in brackets e.g. {1} This makes it easier to locate pins in the symbol editor, even when the names are not intended to be seen in a design. The pin names are selected and then switched off in the **Properties** dialog under the **Pin** page.



Chapter 3. Schematic Design

Unfinished Schematic Connections

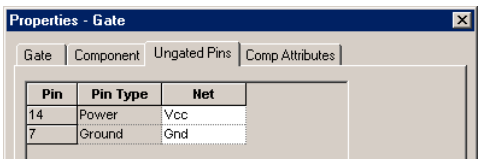
Connections in the Schematic design editor are drawn as **unfinished** if they do not end on an item, or are on a net that contains less than two Component pins. These will also be flagged in the **Unfinished Items Report** and the **Nets Report** as unfinished.

The **Remove Unfinished Connections** option will still only remove connections not ending on an item.

The **Electrical Rules Check - unfinished Connections check** will still only add an error to connections not ending on an item.

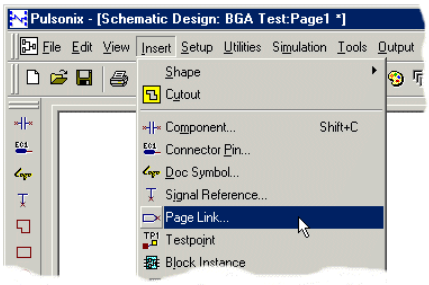
Ungated Pins show Pin type

The **Ungated Pins** page on **Properties** now shows the **Pin Type** defined in the Part, (this is not editable in this dialog).



Insert Page Link

There is a new option **Insert Page Link** on the Schematic **Insert** menu to insert a page link symbol.



When the Schematic Documentation Symbol is created it will include the <Page Link> and <Net Name> attributes by default.

A Signal Reference Documentation Symbol can also contain the <Page Link> attribute if you wish to link to another page from that symbol.

New Default Attribute Available

A new attribute <Block Author> is available for use in the design. Add it using **Insert Attribute** or **Insert Attribute Position** from the **Insert** menu.

The value of this attribute is the same as <Design Author> except when attached to a block instance, it gets the value which was copied from the block design. By changing <Design Author> to <Block Author> in the Schematic profile, you will get the name of the original block author in the appropriate places.

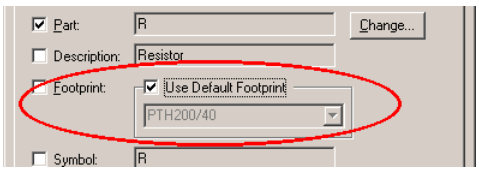
Use Default Footprint in Component Properties

The rules regarding the use of the Default Footprint on a component have been tightened so that if the Footprint is changed from that of the default, other options such as Synchronise Design will know how to react.

Each Part definition can have one or more footprints assigned to it. If you have more than one then the first one in the list (in the Part) will be the default one.

In the Schematic design, the default one is always used as long as the footprint doesn't get changed in the Properties dialog.

A new check box, **Use Default Footprint**, will ensure that the default footprint is always used unless specifically changed by unchecking this option and selecting the new footprint from the drop down list.



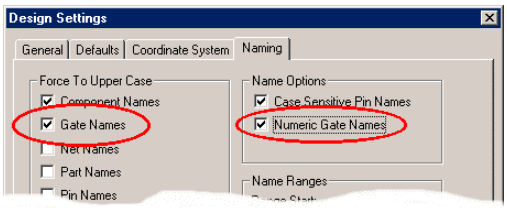
This change affects both the initial **Translate To PCB** option and the subsequent **Synchronise Design** option.

User Defined Gate Modifiers

Previously Pulsonix Schematics only allowed you to use lower case gate letters e.g. IC1-a, U3-c. You can now use upper case letters, or numbers e.g. IC1-A or IC1/1, U3/3 etc.

The Schematic to PCB transfer option will pass these settings across to the PCB design so that back annotation reports from PCB use the correct notation.

To facilitate this, there are two new switches under **Design Settings** and **Naming** page on the **Setup** menu; Upper Case Gate Names and Numeric Gate Names.

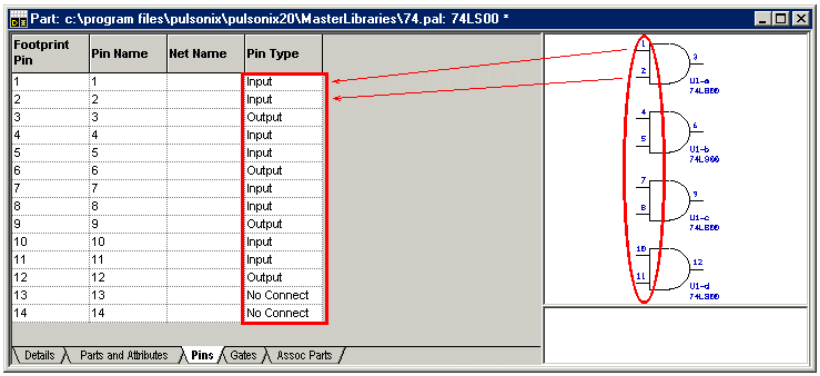


There are also new **Design Settings** dialogs in Part Edit and Part Technology designs to provide these switches for use in the gate page on a Part definition.

Pin Types in Part Editor

Match Pin Types

The new option on the Tools menu, Match Pin Types, makes a rudimentary guess as to what a pin type would be. This is based on the position of the Symbol pin and net names. Pin positions on the left of the symbol are guessed to being Input pins, and on the right side of the Symbol, Output pins. Any pins at the top or the bottom of the Symbol are classed as Input pins. Obviously, any pre-selected pin types can be changed afterwards. This option is there purely to help allocate Pin Types based on its best guess.

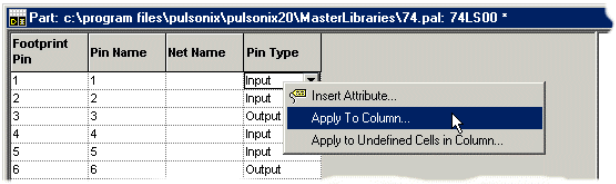


In the example above, after running the Match Pin Types option, the input pins and output pins have been allocated to their corresponding pin types.

Apply to Undefined

Also in the Part Editor on the Pins page, you now have two new options on the right mouse menu, **Apply to Undefined** and **Apply To Column** in the grid.

Apply To Column will apply the current pin type to the whole column regardless of their pin type.



Where any cell of the Pin Type column is marked as **Undefined**, by selecting another defined Pin type first and then right clicking, you can apply that Pin Type to the Undefined ones.

Changes to SCM To PCB and Synchronise Design

On the **Translate To PCB** option, styles on Net Classes may be adjusted to other existing styles to conform to the net class rules defined in the Schematic. If no suitable style is found, a warning is issued. Similarly, when using **Synchronise Design**, Net Classes that have changed will have their styles validated against the rules. This time, no styles are changed and invalid Net Classes are just reported.

Changes to Spice Simulator

New In-built Probe

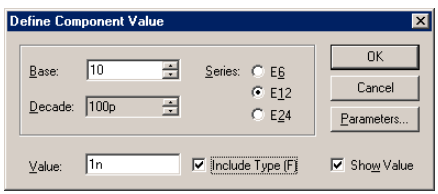
There is a new in-built probe type (and Part) **dB Relative Voltage Probe.** The templates for the **dB** and **Phase Voltage Probes** have been corrected.

New Switches on Edit Dialog

There are new switches on some of the **F7** (Edit Spice Model/Value) dialogs to show the spice value in the design, e.g. for passive devices **Show Value**, and for models **Show Value** and **Show Params**

Spice Capacitor

When editing a Capacitor using the **F7** (Edit Spice Model/Value) option the dialog now has a switch for you to include the F (Farads) symbol after the component value.

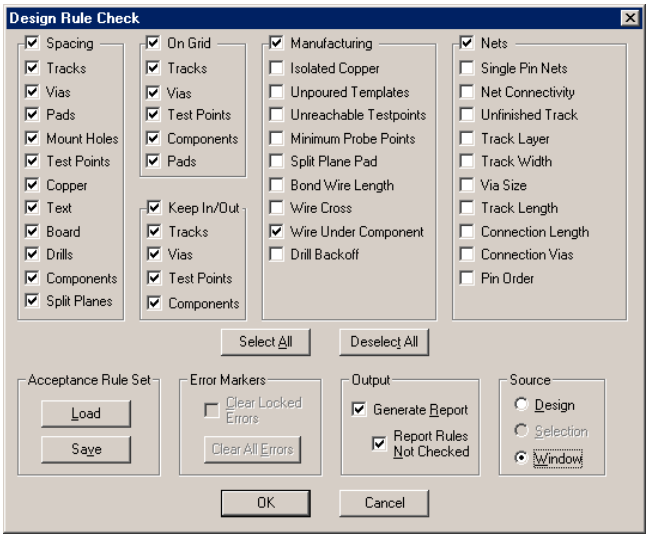


Chapter 4. PCB Design

DRC Changes

New Checks

A new check has been introduced under the **Manufacturing** list for **Wire Under Components**. It is self explanatory but when run, this will report an error if the end of the wire is on a via or pad under a Component. Where jumpers or wire links exist inside the Component bounding box or placement area, these are likely to be unmanufacturable, hence this new check.



Reporting of Net Classes - A list of net classes that have spacing rules defined, and a list of net class pairs that have rules defined are reported in the PCB DRC report. If neither, then this is reported also.

Under (checking) **Source**, a new check has been introduced for checking in the current design **Window**. All items within or crossing the window are checked.

A new option on **Output** allows you to **Report Rules Not Checked**.

The DRC report now looks like this:

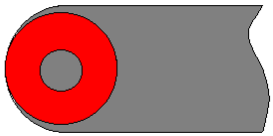
```
No Errors were found

Only checking items in the current window.
```

```
The following rules were not checked:
    Spacing Rules:
        Board (Acceptance Rule)
        Drill (Acceptance Rule)
        Component
        Split Planes
    All On Grid Rules
    All Keep In/Out Rules (Acceptance Rule)
    All Manufacturing Rules
    All Net Rules
Some acceptance rules were not checked.
```

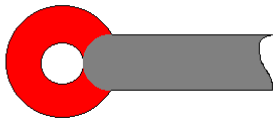
Drill Back-off check

A new manufacturing check has been added - **Drill Backoff**, this reports an error if the pad or via is not big enough for the track to back-off. This check is to ensure that the drill hole does not violate the item being checked against.

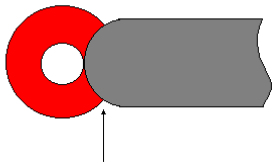


For Track to Drill hole checks the following rule applies:

The resultant effect that will be achieved when the track is backed off during the plotting output stage is shown below:



The problem is when you get a thick track which is much bigger than the pad, the back-off causes the track end to be pulled so far out of the pad (to avoid the drill hole) that there are two small 'cuts' between the track and the pad which can cause 'over-etching' during manufacture.



The diagram above illustrates the area that the over-etching could occur. With larger tracks this is obviously more exaggerated.

When a Track To Drill hole error exists, the track **isn't** backed off during the output stage. In every instance where this situation occurs the edge of the track will be plotted over the pad to the far edge of the pad, covering the drill hole (effectively the same effect as potting with filled pads).

Acceptance Checks

A new option on the DRC/ERC dialogs is for **Acceptance Rule Set**.

The design rule switches that are shown in the DRC and ERC dialogs can now be saved into the design as the 'Acceptance Rule Set'. This is the set of rules that should be checked before the design is to be accepted as complete. The DRC and ERC dialogs still work the same way in that the settings shown in the dialogs are the same as the last time you used them in the current Pulsonix session, but there are now **Load** and **Save** buttons used on the Acceptance Rules in the design.

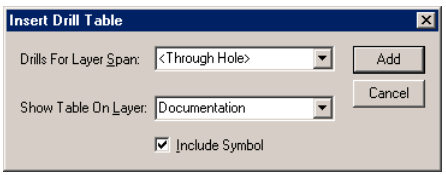
The DRC report says if all the acceptance rules were checked or not.

```
      Spacing Rules:
          Board (Acceptance Rule)
          Split Planes
      All On Grid Rules
      All Keep In/Out Rules (Acceptance Rule)
  Some acceptance rules were not checked.
```

You can now run the Acceptance Rules for DRC and ERC from a user-defined report created in the **Report Maker**. See the section under the *General Options* chapter for the *Report Maker*.

Improved Drill Table detail

A new switch on the **Insert Drill Table** option allows you to **include** the **Symbol** into the table.



When added to the design, the drill table now looks like this:

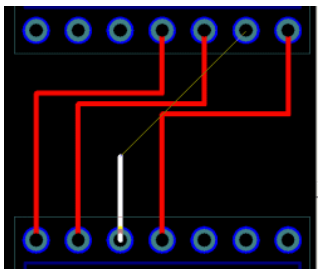
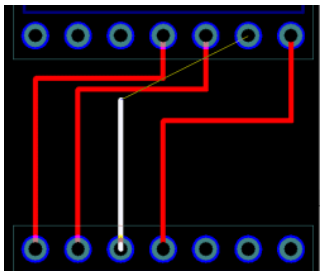
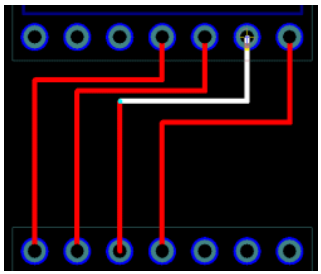
Diam (thou)	Qty	Id	Plated	Symbol
10.0	212	A	x	
28.0	2	D	x	
30.0	2	E	x	
125.0	1	AC		

This switch also applies to the table **Properties** when editing it.

Track Pushing

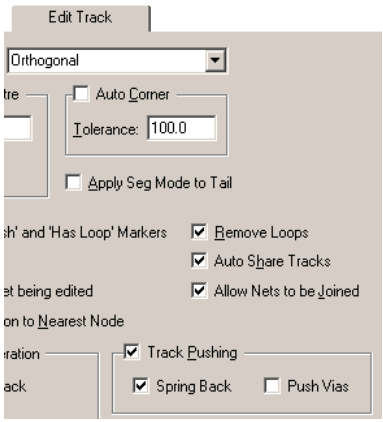
Track and via pushing has been added to Pulsonix PCB. Track pushing is used when a number of existing tracks need to be 'nudged' to make space for a new track being added or edited in the design. Where Online DRC is also enabled, this makes it ideal for packing tracks together using their track-to-track spacing values and for getting the tracks as close to pads as possible, again using their track-to-pad spacing values.

It should be noted that track pushing only works when editing or adding tracks, it doesn't work when moving Components that have tracks attached to them.

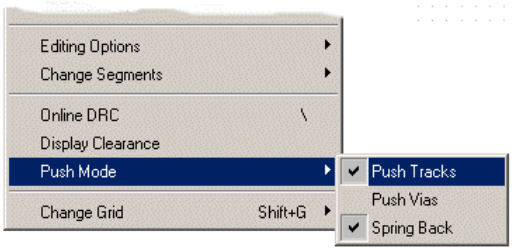
When adding, editing or moving a track segment, existing tracks may get in the way. With **Track Pushing** enabled, nearby existing tracks are *Pushed* away from the track being edited, making design rework much easier. The pushed tracks are *frozen* at their current location when a corner is added and the pushing begins again. Only a limited amount of effort is applied to the pushing, as it is not desirable for a small track modification to push tracks across a large area of the design. With **Online DRC** enabled, the pushing will not introduce design rule errors, othe6rwise tracks may be pushed over other items, causing errors.

There are three new options: **Track Pushing**, **Via Pushing** and **Spring Back**. These can be set up using the **Options** dialog and **Edit Track** page.



When **Spring Back** is enabled, pushed tracks will move back to their original position as the edited track is move away. **Spring Back** is recommended. It is also possible to push vias using the **Push Vias** option. This option will allow vias to be moved, you should be aware that moving a via may make it necessary to rework tracks on other layers.

All of these options are also available from the context menu during the track editing operation.



Cloning styles of existing Tracks

There is a change to the way in which **Tracks**, **Breakouts** and **Wires** can take the default or starting style by using an existing item to clone.

If another track (or breakout) is pre-selected, then the width and layer is taken from the selected segment to use when adding the tracks in this session. This is the same as changing style prior to adding the new track.

Also, if a new net is created for the new track, it will use the net class from the pre-selected track. The pre-selected track will remain selected until the first track is added.

Note: this behaviour does not happen when you double click on a pad in select mode.

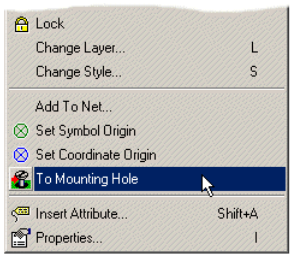
The **Insert Wire** command will copy the insulated flag as well.

Unpoured active templates included in Completion report

The **Net Completion** report now includes unpoured active templates to give a more comprehensive and accurate report of completion.

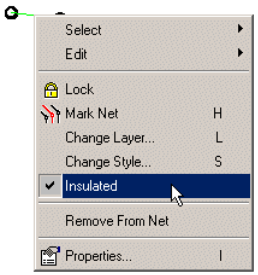
New ‘To Mounting Hole’ command

A new command To Mounting Hole exists in the PCB Footprint editor. This is used on a selected pad to convert it to a mounting hole. When used, it renumbers the appropriate pads back in sequence. Particularly useful on converted libraries from other systems that do not have a mounting hole concept.



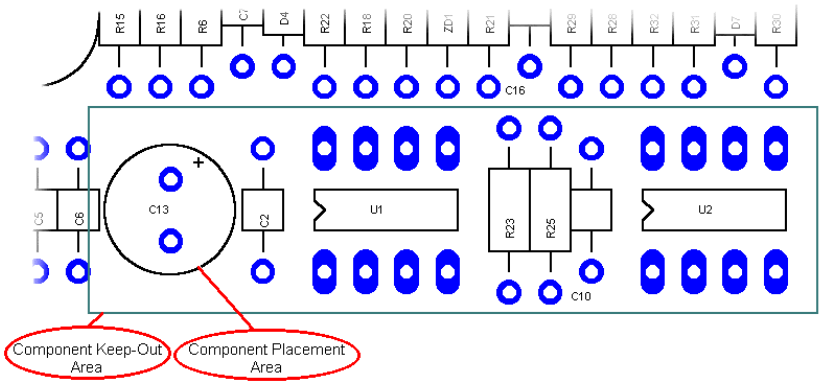
New ‘Insulated’ command

When editing or adding a wire to a design or footprint library item, if you right click, the content menu now has a command, **Insulated** to toggle the wire Insulated state. Only non-insulated wires are checked for cross when using DRC.



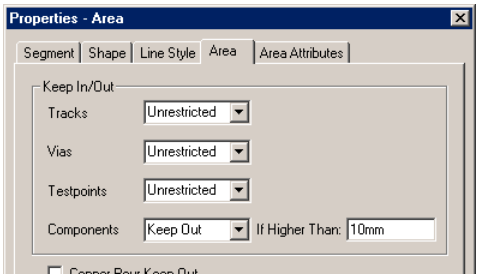
Component Height Checking

You can now set a height on a component, and set a maximum height on a Component Keep-out area in the design. The Design Rules Checking option will report errors where Components are too high to fit in the area. The Component can have a height attribute, or it can have height attributes set its areas. This way different areas of the same Component can be set with different heights.



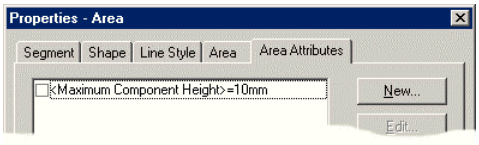
To use this facility you must first add an **Area** to the design first.

Use **Properties** of the area by selecting it and right mouse clicking. On the **Area** page, change **Components**: to **Keep Out**. You will then be able to enter a value for **If Higher Than**:

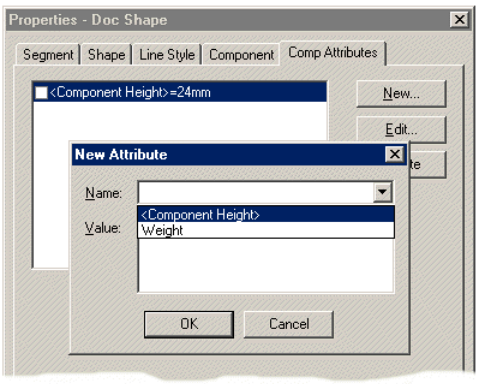


Alternatively, you can select the **<Maximum Component Height>** attribute from the **Area Attributes** page of the **Area Properties** dialog. You must also type in a Value for this attribute.

If you went through the Area page as above, the <Maximum Component Height> attribute and value would automatically be filled in for you.



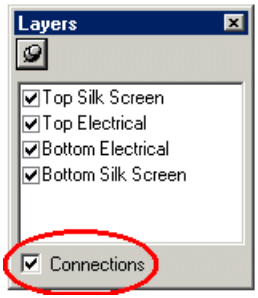
On the Component itself, you can edit this <Component Height> on the Comp Attributes page. This attribute is built in and is shown in chevrons.



You can also set an area on a Component to Keep Out Components higher than a value. This allows you to set the placement height of a comp to be 12mm for example, but have an area in the middle that keeps out components greater than 8mm. So flat components with a height less than 8mm will legally fit under the original component.

Changes Layers On/Off Bar

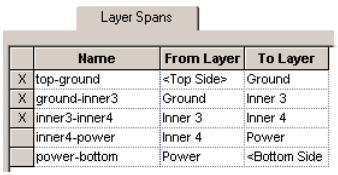
The Layers browser now includes a **Connections** check box to toggle connections on and off.



Via Spans

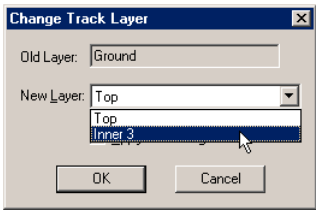
The use of via spans has been improved so that where complex via spans are being used through-hole vias are not introduced accidentally.

For example, the **Technology** file **Layer Spans** might look like this:



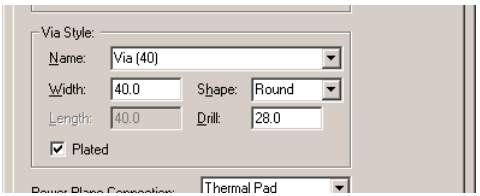
	Name	From Layer	To Layer
X	top-ground	<Top Side>	Ground
X	ground-inner3	Ground	Inner 3
X	inner3-inner4	Inner 3	Inner 4
	inner4-power	Inner 4	Power
	power-bottom	Power	<Bottom Side

When using manual routing in the PCB design, once you get into the inner layers, only legal and viable via spans are presented to you in the **Change Layer** dialog.



Plated flag available in Properties

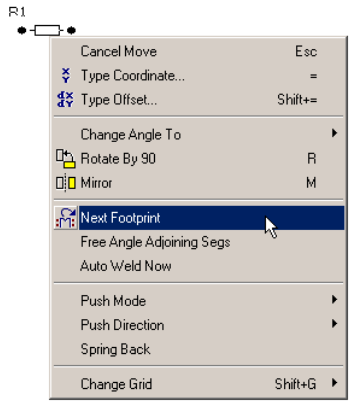
You can see and edit the **plated** flag on pads and vias. This is useful for checking the plate status of vias and mounting holes.



Next Footprint

During Insert, Move or the selection of a PCB Component, there is a new option on the context menu called **Next Footprint**. This is only available if the Part has more than one alternative footprint defined for it. This changes the footprint to the next one in the list, and toggles round the full list.

This option can also be assigned to a shortcut key if required.



Gate & Pin Swapping in Specctra

Part information is now output to Specctra. This means that any Gate & Pin swaps performed in the Specctra router are imported back into Pulsonix.

Extended Select

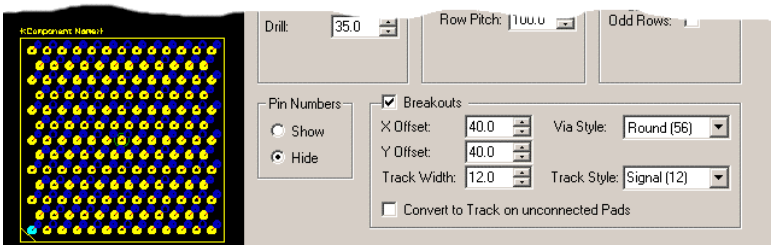
Shift select on a connection in the PCB design editor now selects all of the connections on that net. Previously this didn't happen.

This mechanism also works for Breakouts and Wires.

Breakout changes

Footprint Generator

From the **Pads** page of the PCB Footprint Wizard, you are now able to generate a single segment **breakout** on each pad of a BGA.



The **X Offset** and **Y Offset** allow you to create the direction of the breakout. The value entered in these boxes can be positive or negative numbers depending on the direction required. You can also specify the **Track Width** and **Style** required for the breakout as well as the **Via Style** if you wish to end on a via.

The check box to **Convert to Track on unconnected Pads** is a property of the breakout. This is an existing property available in the footprint editor also.

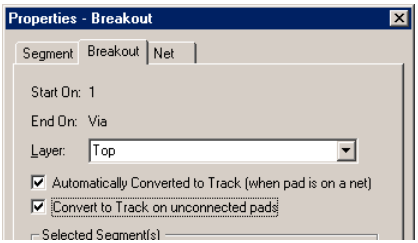
New Switch on Design Settings

Under the **Setup** menu and **Design Settings**, on the **General** page there is a new switch **Allow PCB Only single pin nets**.

This allows the creation of single pin nets, even if netlist changes are not allowed. When performing **Synchronise Design** these single pin nets will be ignored. This is useful for adding single pin net test lands or for thermal balancing, where otherwise unconnected pads need to be routed. Like the **PCB Safe Mode** (detailed below), this switch can be set up in the Schematics and passed to the PCB design.

Breakout Properties

When using **Properties** on breakouts in a Footprint, there is a new switch **Convert to track on unconnected pads**. Use this to create PCB only nets on unconnected pins when using the **Convert Breakouts to Track** mode in the PCB design.

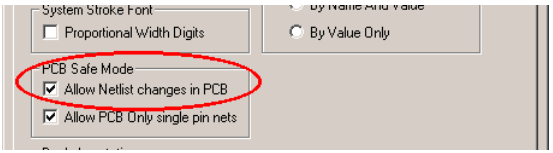


*Note: These will get ripped out when using **Synchronise Design** if the switch in **Design Settings** (**Allow PCB Only single pin nets**) is not set on.*

Changes to PCB Safe Mode

This switch has been moved from the **General** options page of the **Options** dialog to the **General** page of the **Design Settings** page.

This change means that the status of the switch is now held in the design (and technology files) rather than saving it in the registry as it was previously.



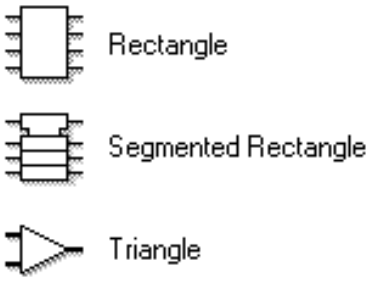
These options can now be set up in the Schematic design, so that the engineer can control the changes that the PCB designer can make later on. (The Schematic settings are the defaults passed to the new PCB design but they can still be overridden in the PCB design, if necessary).

Chapter 5. Library Toolkit

New Symbol Definition

The Library Toolkit option now contains a new section for the generation of Schematic Symbols in addition to the existing PCB Footprints and Parts.

New Symbol shapes can be added for Rectangle, Segmented Rectangle and Triangle:



The new file definition is documented in the **Library Toolkit users guide** supplied on the installation CDROM under \Documents.

Appendix A Default Files

This section details new default files supplied or changes made to existing files.

Technology Files

Schematic Technology Files (*.stf)

All Schematic technology files have been modified so that **Unconnected pins** are shown **on** by default and **Connect Points** for Symbols are **not** shown. The effect of this is that until the pin is connected to, it is displayed, once connected to, it is switched off.

Format Files

New format file(s) for version 2.1 include:

- **IPC-356_full.rff** — Output formatter for the IPC356 test format. Uses all pads and vias for test lands, not just nominated Testpoints.
- **Schematic Acceptance Report.rff** — Output formatter for running ERC option from within Report Maker option.
- **PCB Acceptance Report.rff** — Output formatter for running DRC option from within Report Maker option.

Both acceptance report formatters show off new features for running reports within reports, running ERC and DRC options, Boolean variable and Is Bin Empty command.

Colour Files

As with the Colour settings in Technology files, all Schematic Colour files have been modified so that **Unconnected pins** are shown **on** by default and **Connect Points** for Symbols are **not** shown. The effect of this is that until the pin is connected to, it is displayed, once connected to, it is switched off.